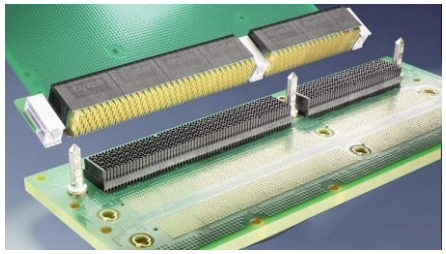
Embedded Tech Trends 2014

January 20, 2014

The Rising Importance of Signal Integrity in VPX systems



Matt McAlonis- Development Engineering Manager

EVERY CONNECTION COUNTS

TE connectivity

Consumer products world…

“Don’t take it serious…
live and laugh at it all…”

“a bowl of cherries”

Telecom Products World…

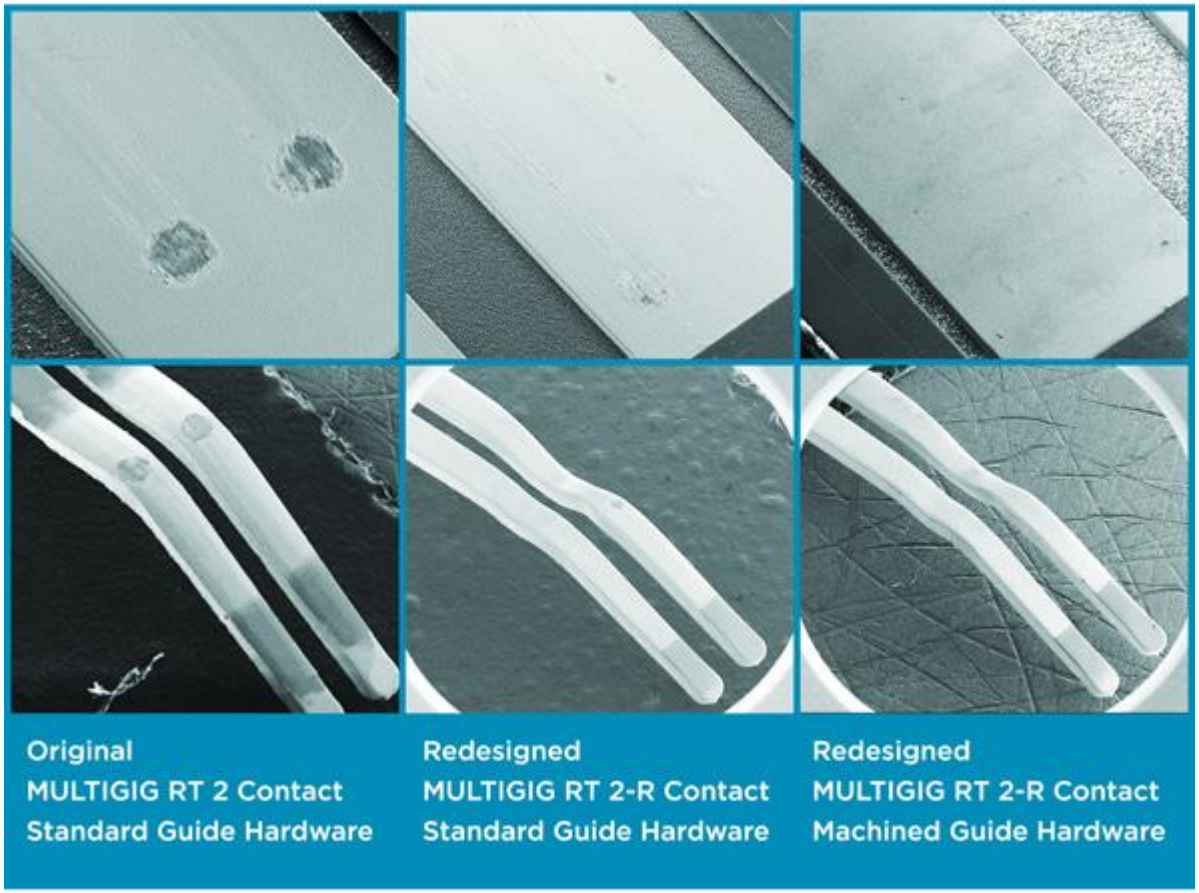
"a box of chocolates"

Embedded Computing world…

“What we do today, might burn us tomorrow…”

“jar of jalapeños”

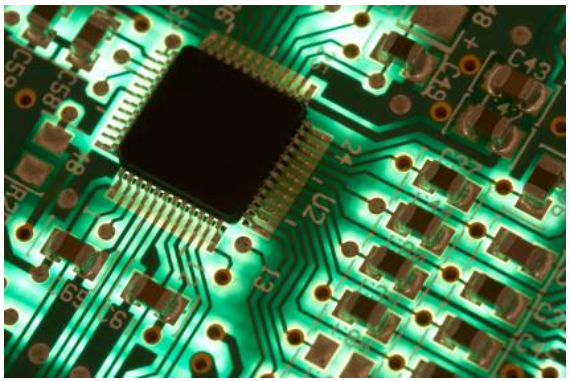
Last year at ETT…

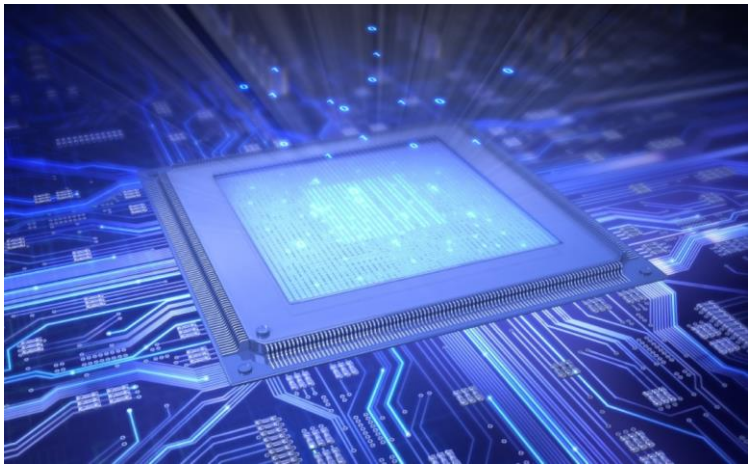


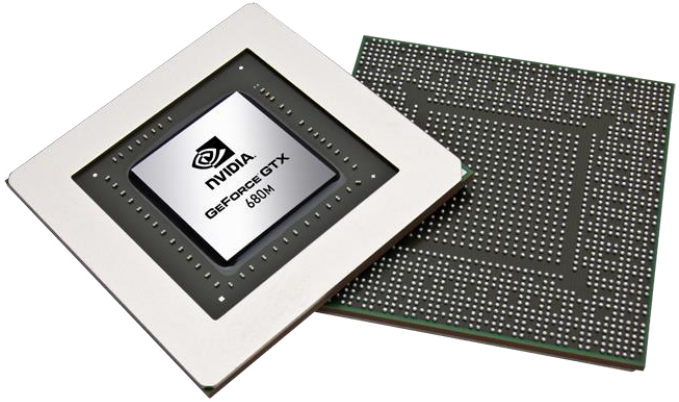
Expanding a strong foundation of rugged VPX products with RT 2-R

The World of rapidly evolving high performance computing

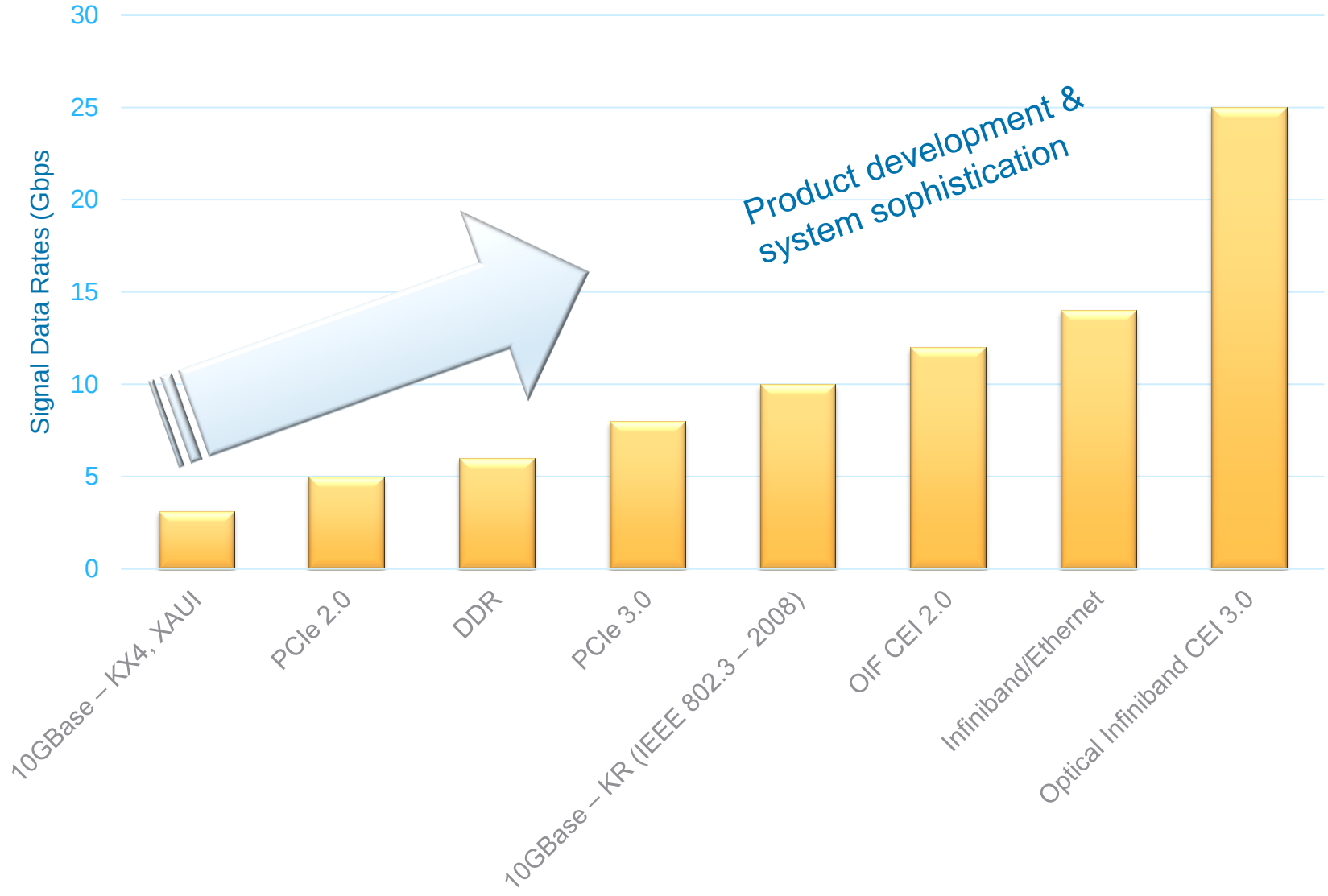
- CPU's, GPU's, & FPGA's



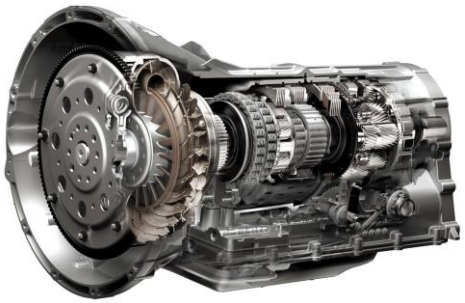




Protocols and Data Rates

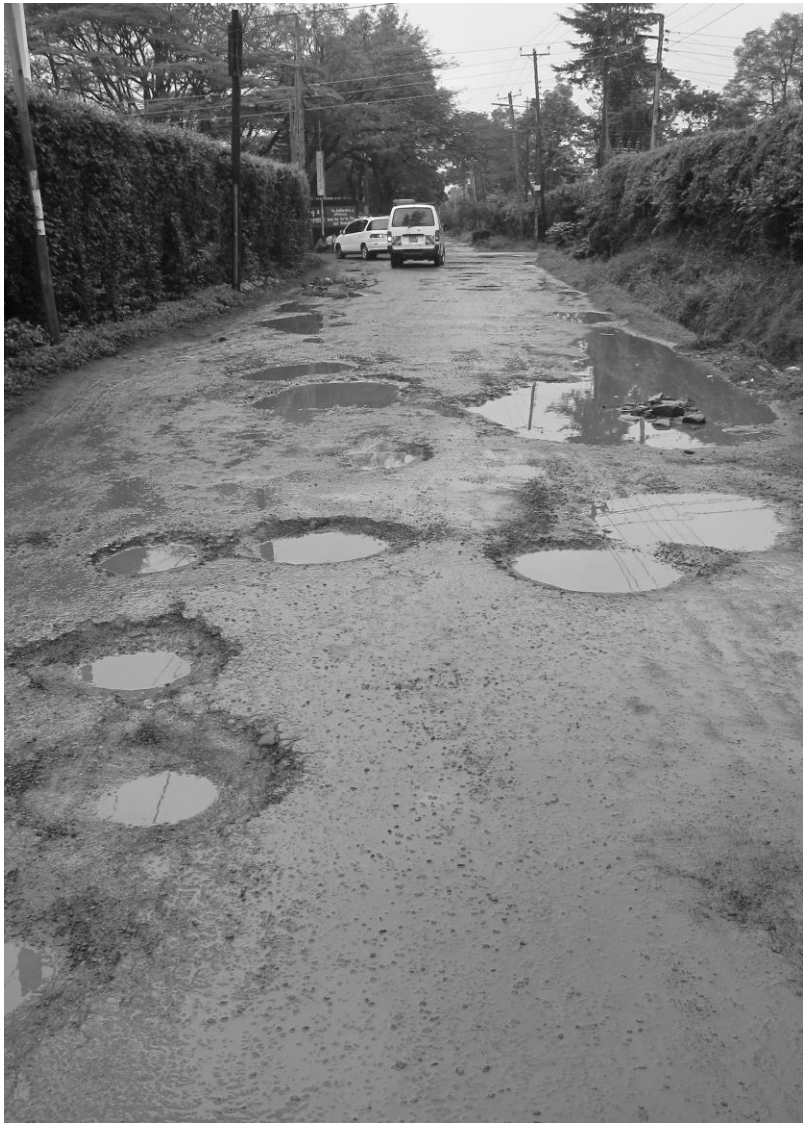


System performance depends on…

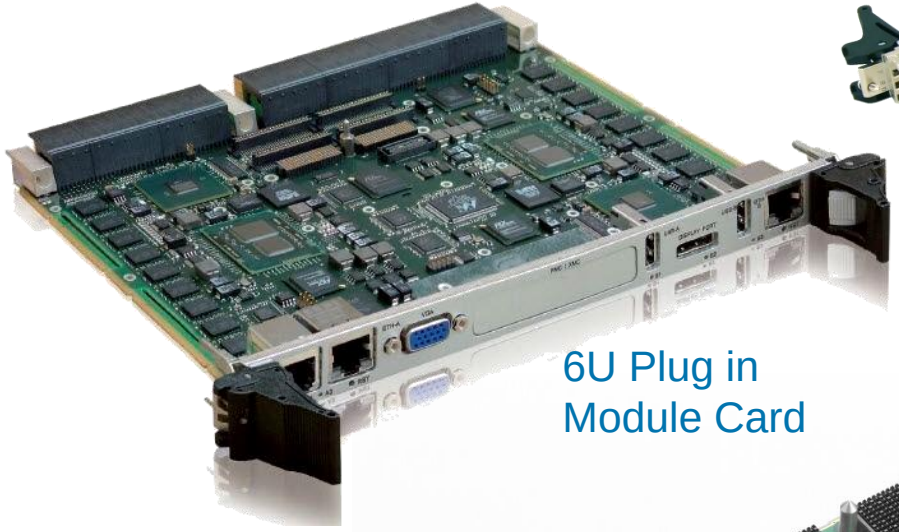


What is the path of the circuit

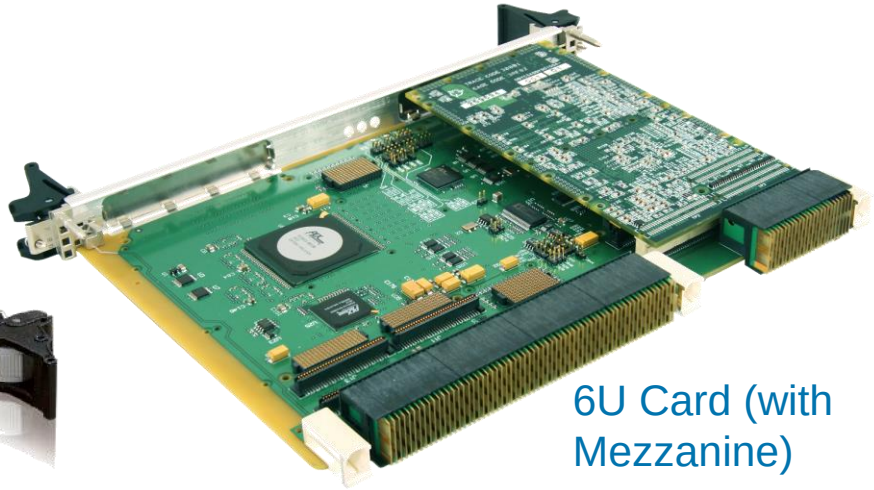
What is the environment



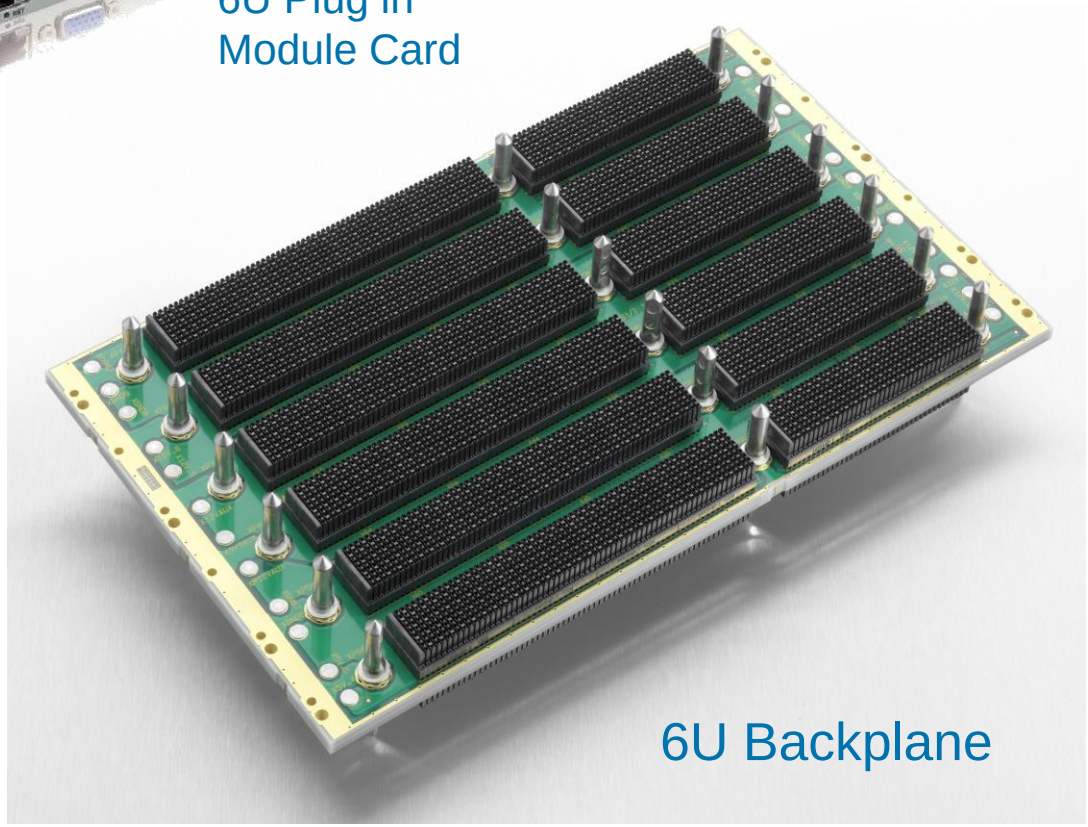
VPX Products



6U Plug in Module Card

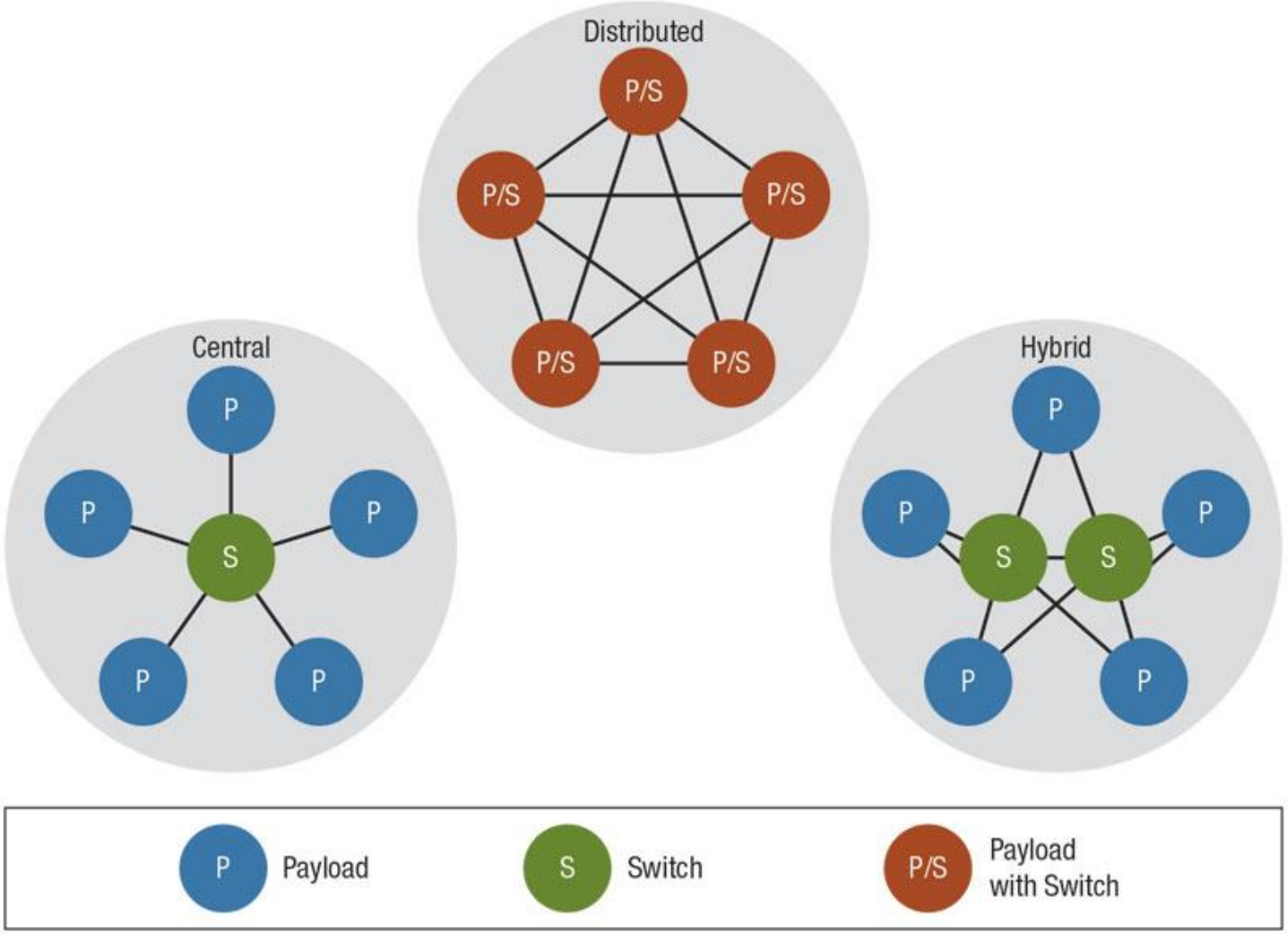


6U Card (with Mezzanine)

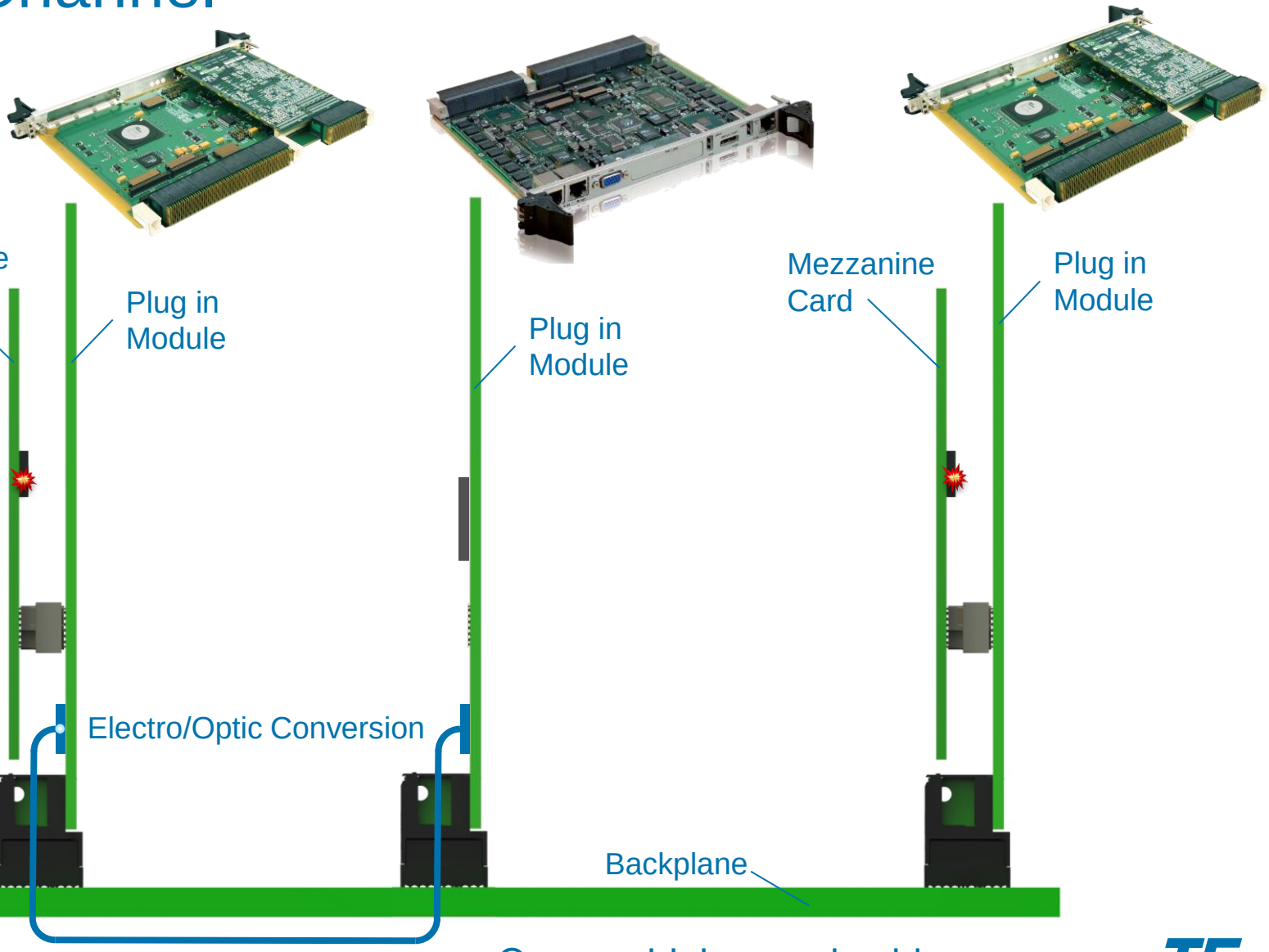


6U Backplane

VPX Backplane Topologies



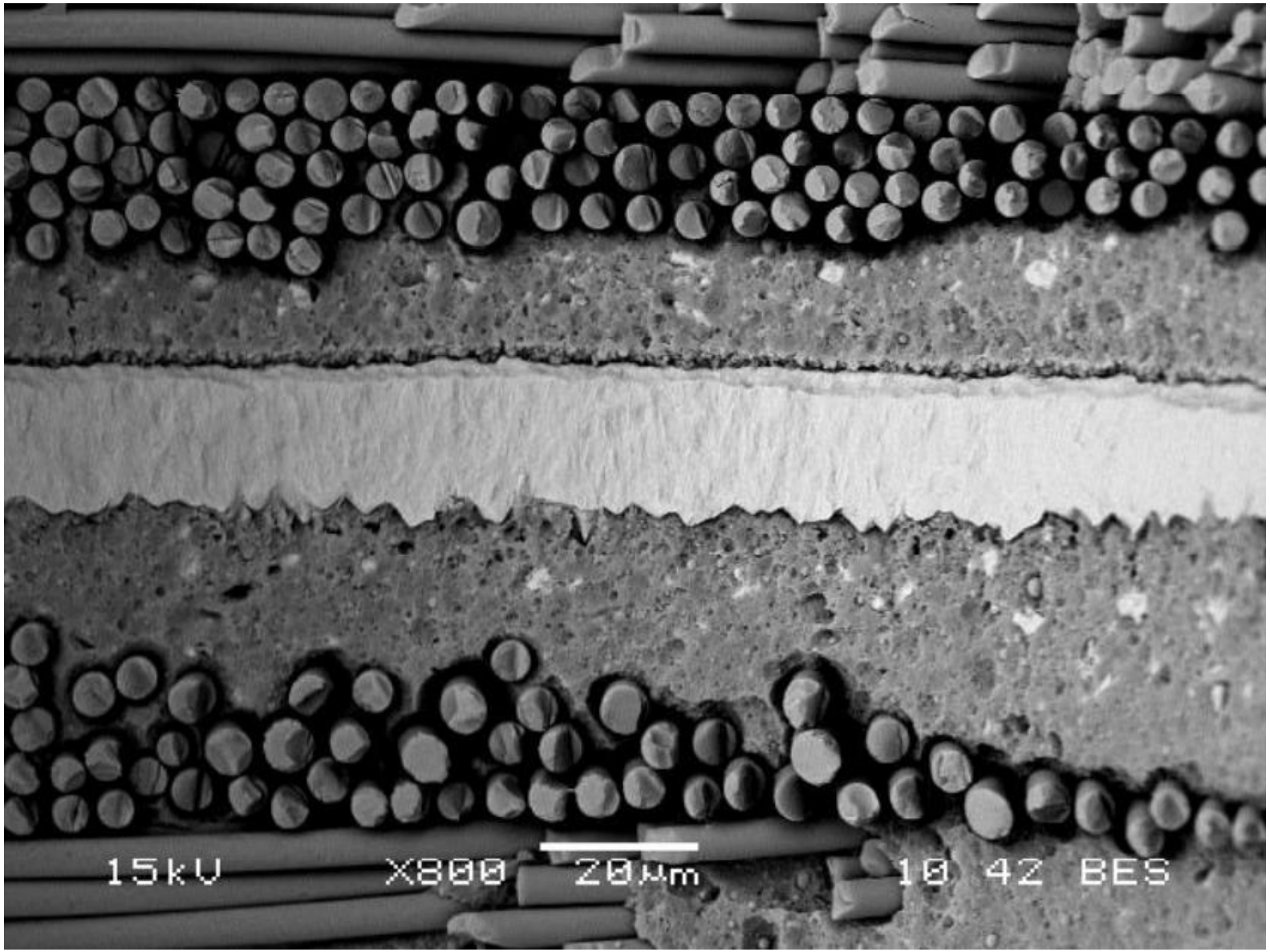
VPX Channel



Or even high speed cable…

Take Nothing for Granted

- Design Analysis
  - 3D Electromagnetic solvers, S-parameter characterization
- Connections
  - Improved connector footprints and via optimization
- Manufacturing
  - Better PCB materials & no-stub techniques
- Backplane
  - Data flow architecture and high speed routing rules
- Silicon Technology
  - Passive & Active signal conditioning, multi-level encoding
- Equalization Techniques
  - Decision feedback equalizer (DFE) & Forward Error Correction (FFE)


15kV X800 20µm 10 42 BES

Copper Foil Definition

Shiny Cu

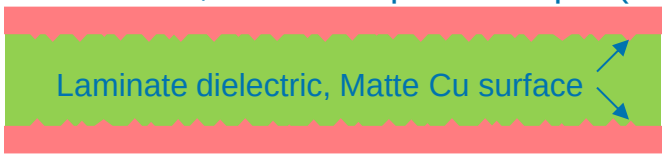
- Matte (opposite drum side) **towards** laminate
- Shiny drum side towards prepreg

Standard Cu (S)

- IPC-4562A, no roughness designation

Low Profile and Very Low Profile Cu

- a.k.a. L or LP and V or VLP
- IPC-4562A, Max. LP profile 10.2µm (400 µin)
- IPC-4562A, Max. VLP profile 5.1µm (200 µin)



Ultra Low Profile Cu

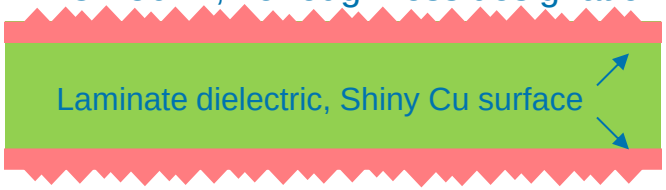
- a.k.a. HVLP, VSP, VLP2, HSVSP, etc.
- IPC-4562A, No treatment or roughness

Reverse Treat Cu

- a.k.a. RTF, RTC, DSTF
- Matte (opposite drum side) **AWAY** from laminate
- Shiny drum side towards laminate

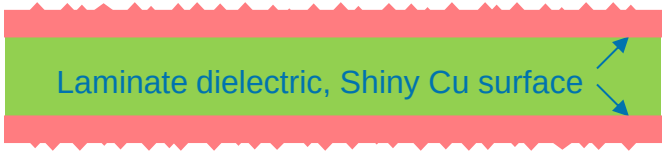
RTF Standard Cu (S)

- IPC-4562A, no roughness designation



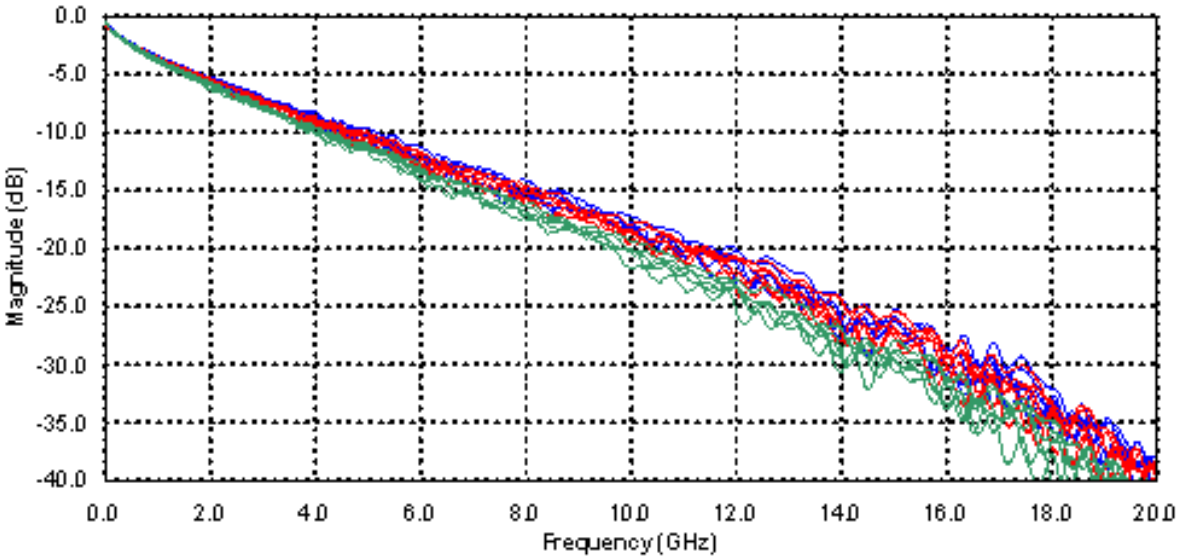
RTF VLP Cu

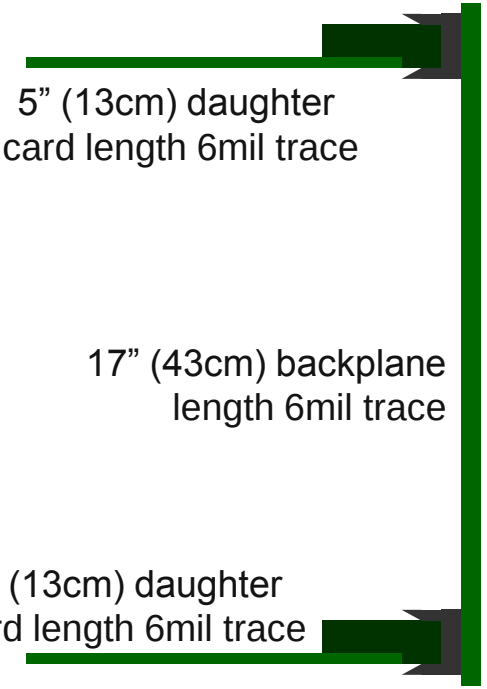
- IPC-4562A, Max. LP profile 10.2µm (400 µin)
- IPC-4562A, Max. VLP profile 5.1µm (200 µin)



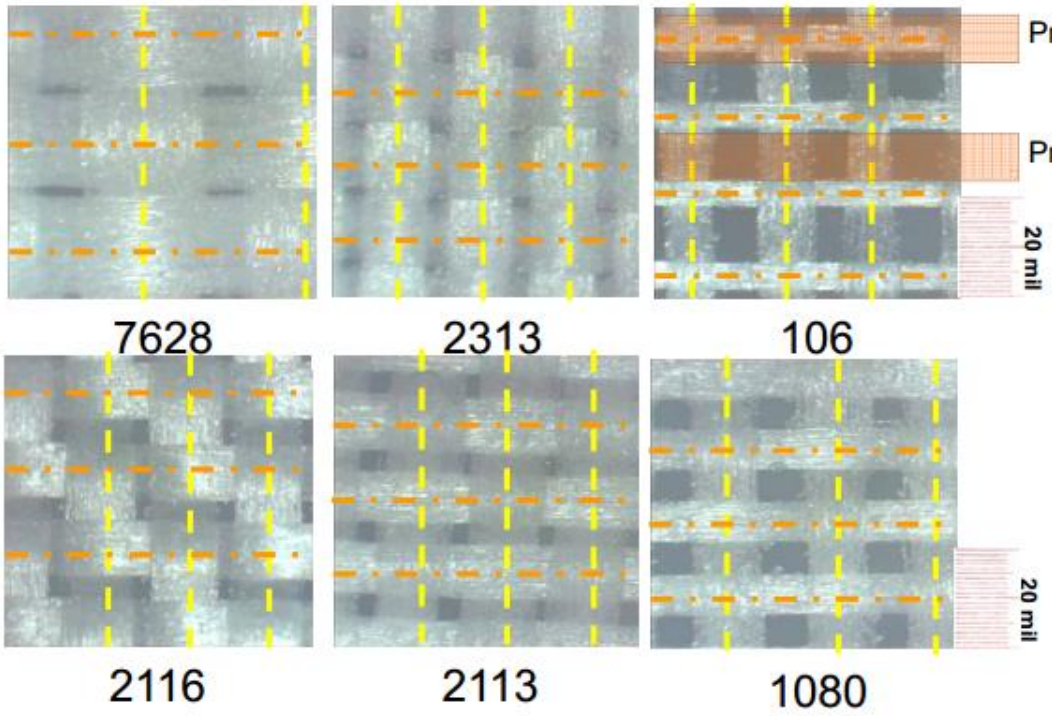
Typical Backplane Channel Insertion Loss

PCB Material	Loss/in	Loss @ 27” (0.7m)	Length @ -25dB
Megtron 6 HVLP	**0.75 dB/in**	**20 dB**	**33” (0.8m)**
Megtron 6 HTE	**1.0 dB/in**	**27 dB**	**25” (0.6m)**
Nelco 4000-13SI	0.9 dB/in	24 dB	28” (0.7m)





PCB Glass Weave effects



FR4 Dielectrics

ε_r (Glass) ≈ 6.0 – 7.0

ε_r (Resin) ≈ 2.5 – 3..5

$Z_0 \approx \frac{1}{\sqrt{\varepsilon_r}}$ $t_{pd} \approx \sqrt{\varepsilon_r}$

Z_0 (Glass) Lower

Z_0 (Resin) Higher

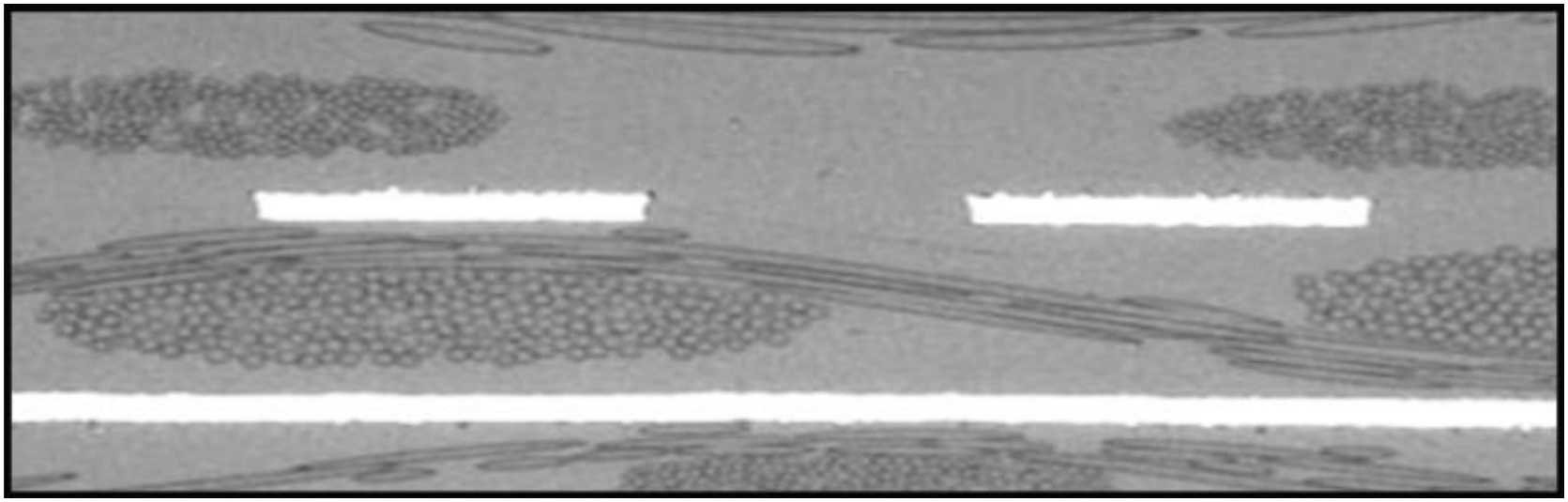
t_{pd} (Glass) Higher

t_{pd} (Resin) Lower

SANMINA-SCI

TE connectivity

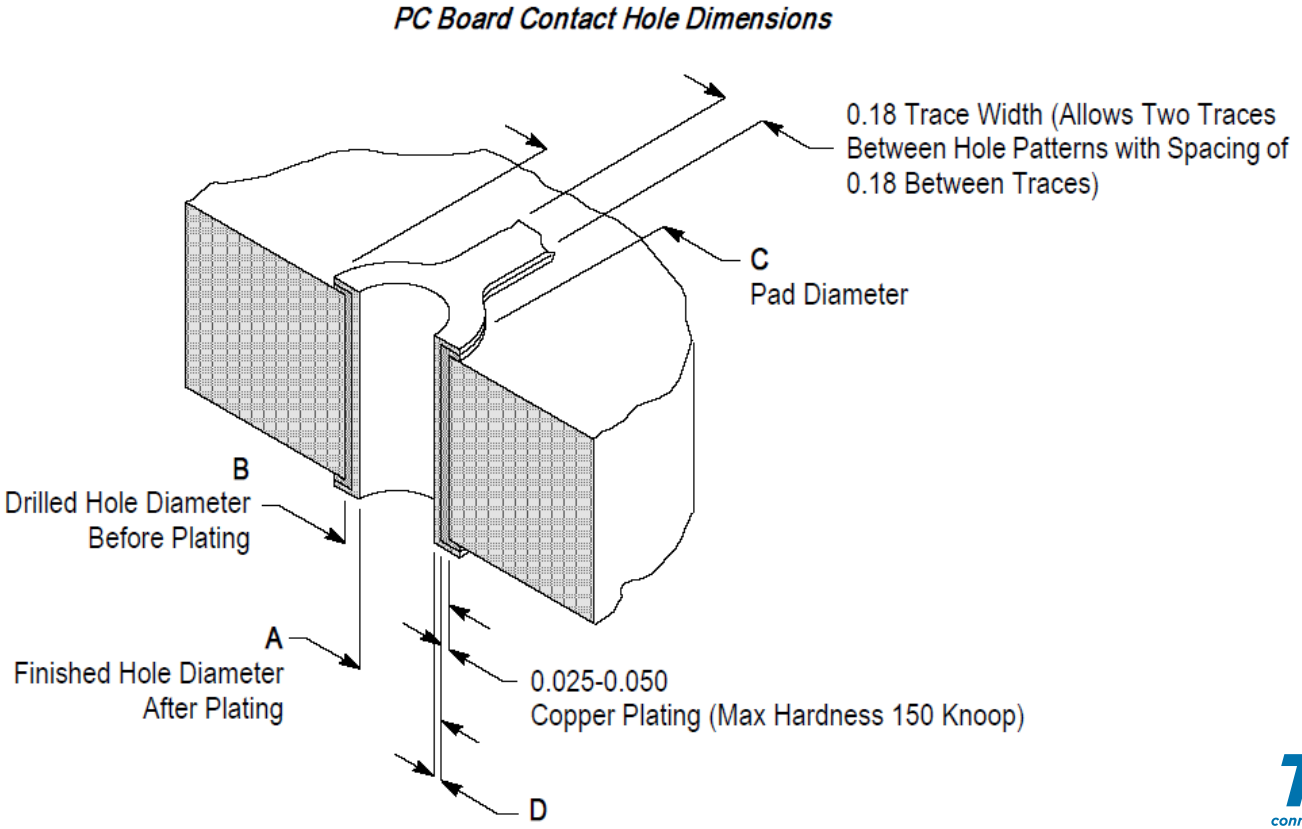
Differential Signal pair



Cross section view of a differential signal pair with varying levels of fiber weave effect

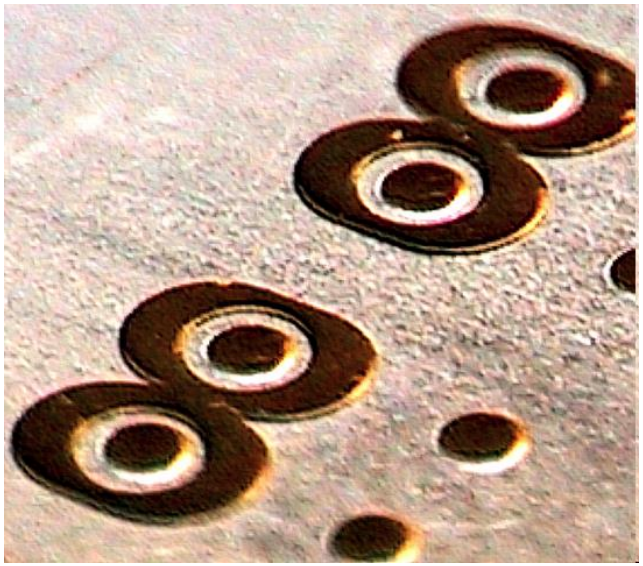
High Speed Design Rules

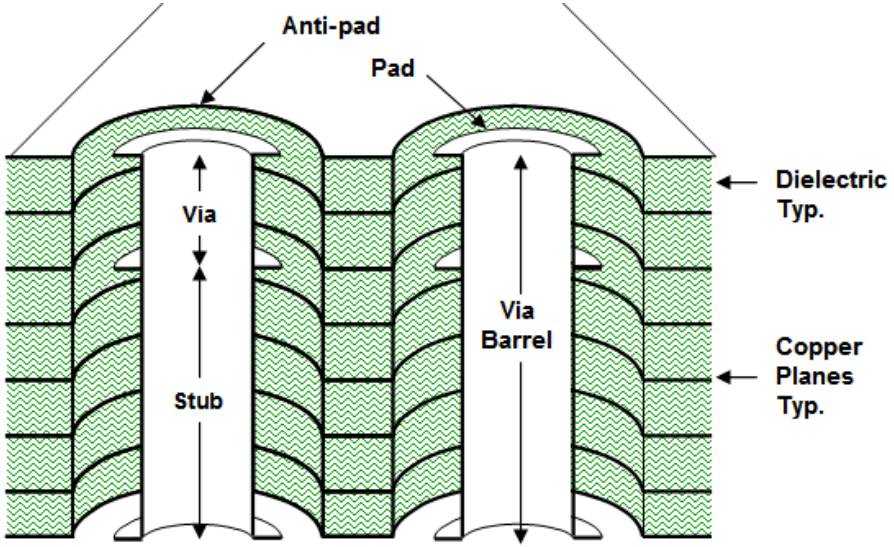
- PCB Fab technology
  - Materials- (many choice$)
  - Via tolerances (**must** be compliant to MULTIGIG RT 2 App Spec 114-13056)
    - *Drill* (most important, never compromise!)
    - Cu
    - Finish

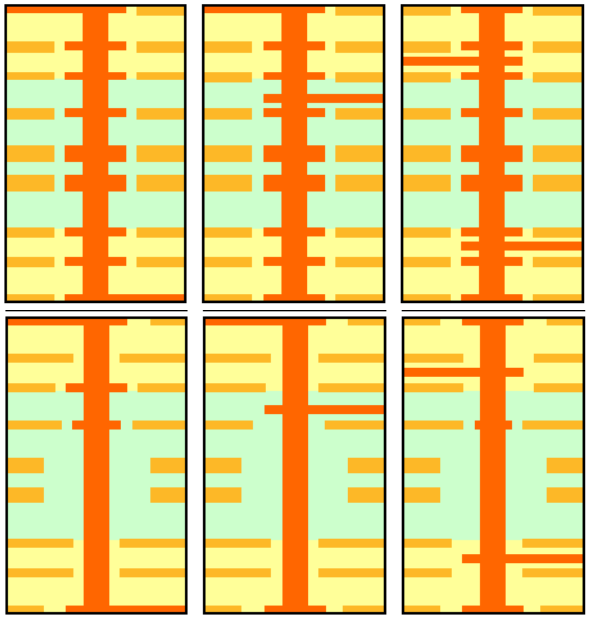


High Speed Design Rules

- PCB Fab technology
  - Pad sizes
  - Non-Functional Pads
  - Antipads
    - Size
    - Shape







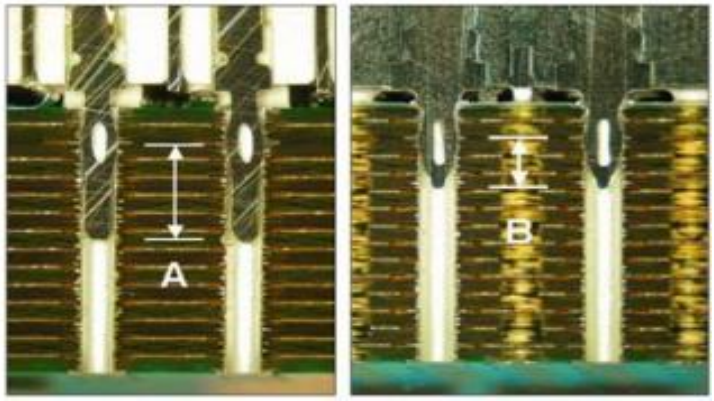
"Standard"

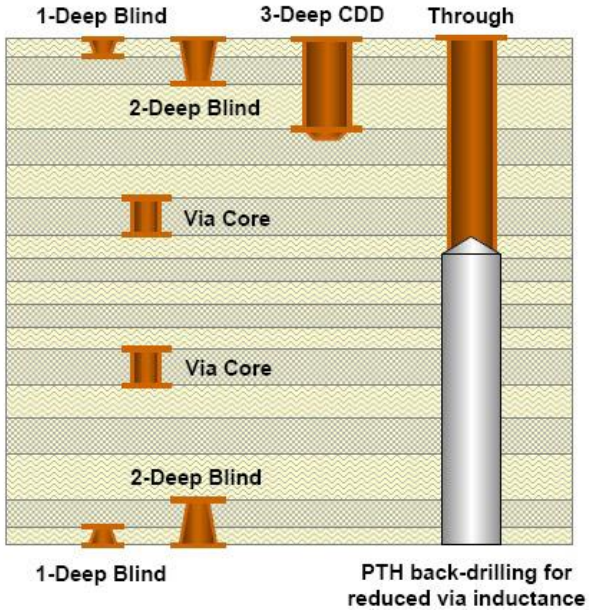
Optimized
- Min diameter
- Eliminate non-functional

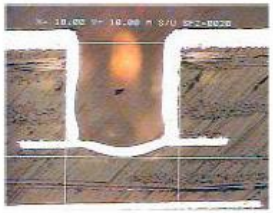
TE connectivity

High Speed Design Rules

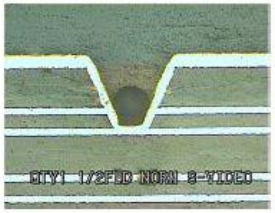
- PCB Fab technology
  - Via Stub Control
    - Counterboring
    - Controlled Depth Drilling
    - Blind Vias



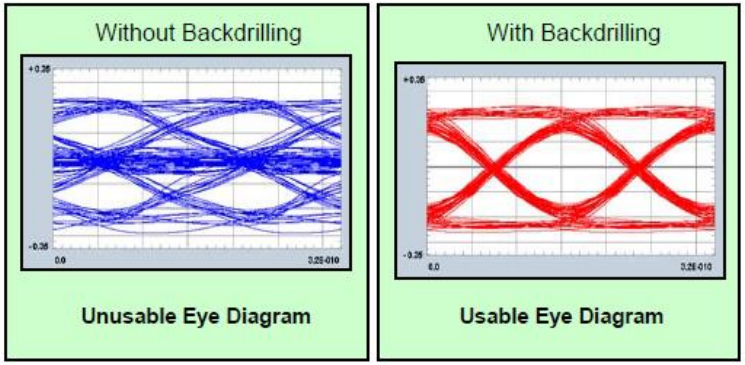




10 mil via 10 mil Deep Layer 3 connection



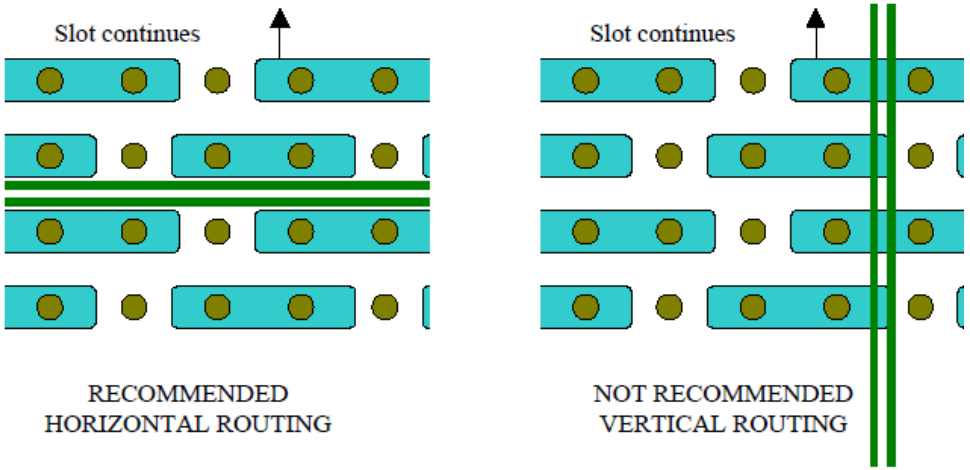
Shaped 6 mil drill

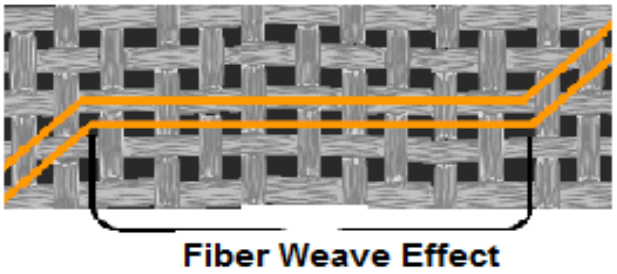


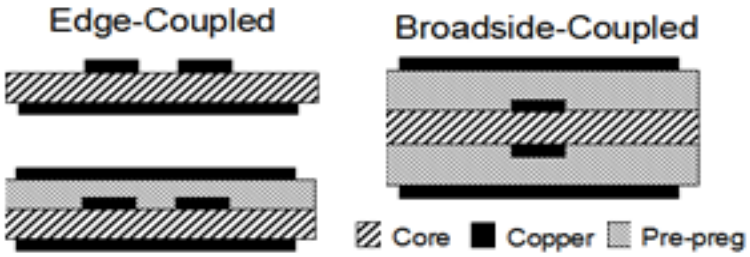
6.25 Gb/s data rate

High Speed Design Rules

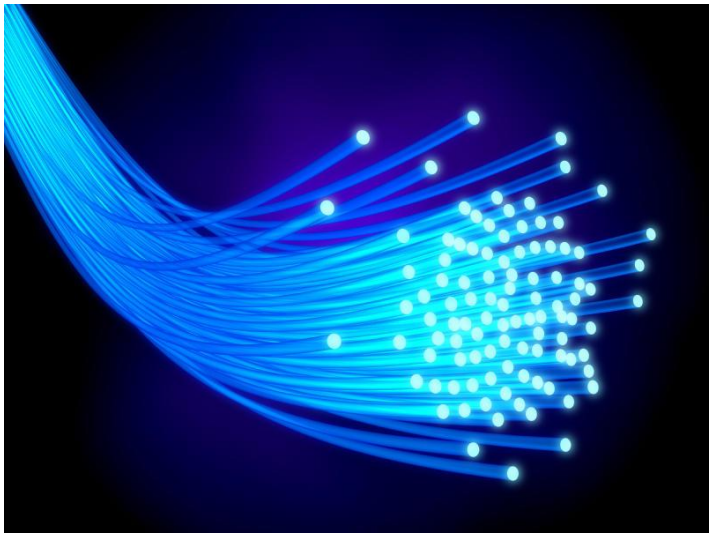
- PCB Fab technology
  - Routing Channels



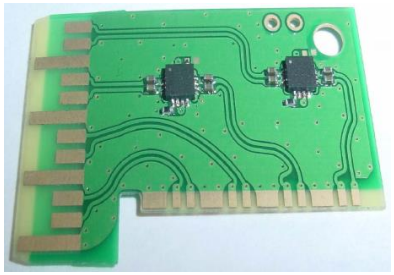


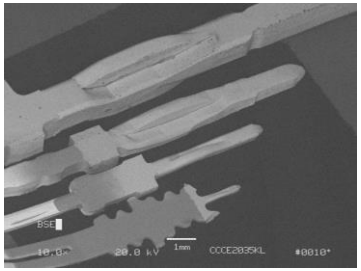


Embedded Tech Trends in VPX



- Where things are going…
- Performance and reliability matters
- What can we do about it?
  - VITA 46 compliance
  - Leap to alternate technology (F/O, etc.)
  - Intermateable VPX derivatives with enhanced performance





- Know what we really **need**…Everything Matters!

Readily Available studies on Via design for High Speed Signaling

- Agilent EEsof EDA, Presentation Designing a Transparent Via, 2007
- DesignCon 2012 - Vias, Structural Details and their Effect on System Performance
- UltraCAD Design Note – The Effects of Vias on PCB Traces
- Ravi Kollipara & Ben Chia – Modeling, Verification of backplane Press-fit Vias
- Lambert Simonovich, Dr.Eric Bogatin & Dr. Yazi Cao – Method of Modeling Differential Vias
- Sanmina SCI
- And many more ……..

EVERY CONNECTION COUNTS